REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-129, 133, 134, 135, 139, 140, 143, and 150-174 remain active in this case, Claims 130-132, 136-138, 141-142 and 144-149 having been canceled; Claims 120, 121, 123, 125, 127, 129, 133, 139, 143 and 150 amended, and Claims 151-174 added by way of the present amendment.

In the outstanding Official Action, the application was objected to under 37 CFR §1.172(a) as lacking the written consent of all assignees owning an undivided interest in the patent; the drawings were objected to; Claims 102 and 139 were objected to as including informalities requiring correction; the reissue oath/declaration was objected as being defective; Claims 1-150 were rejected under 35 USC §251 as being based upon a defective reissue declaration; Claims 1-150 were rejected under the judicially created doctrine of double patenting over claims 1-20 of U.S. Patent No. 5,521,865 to Ohuchi et al; Claims 130-132, 136-138, 141-142 and 144-149 were rejected under 35 USC §251 for lack of defect in the original patent; and lack of error in obtaining the original patent; Claims 130-132, 136-138, 141-142 and 144-149 were objected to as not drawn to the original species elected in the original patent; Claims 121-129, 134-135 and 140 were rejected under 35 USC §112, first paragraph as containing subject matter which was not described in the specification; Claims 120-129, 133-135, 139-140, 143 and 150 were rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention; and Claims 1-16, 19-32, 35-38, 51-

64, 67-82, 85-100, 103-116 and 119 were rejected under 35 USC §102(e) as being anticipated by Mehrotra et al.

In response to the first paragraph at page 2 of the outstanding Office Action, submitted is the original U.S. Letters Patent consistent with 37 CFR §1.178(a).

In response to the objection under 37 CFR §1.172(a), attached hereto is a "Consent of Assignee" form in compliance with 37 CFR §1.172.

In response to the objection to the drawings, submitted herewith is a separate letter requesting approval for drawing changes, and particularly requesting approval for changes correcting the informalities identified in Figures 23, 29 and 32.

In response to the objection to claims 120 and 139, the informalities identified have been corrected herewith.

In response to the objection to the reissue oath/declaration, it is respectfully requested that the requirement for a substitute declaration be held in abeyance until such time as the present application is allowed.

In response to the outstanding double patenting rejection, submitted herewith is a Terminal Disclaimer disclaiming the terminal portion of any patent which may issue from the present reissue application and which would extend beyond the term of U.S. Patent 5,521,865.

In response to the rejection of claims 130-132, 136-138, 141-142 and 144-149 under 35 USC §151, these claims have been canceled and therefore all outstanding issues in regard to these claims are moot.

In response to the rejection of claims 121-129, 134-135 and 140 under 35 USC §112, first paragraph, Applicants respectfully traverse this rejection because Applicants' disclosure

does provide support for the "binary data latch circuits" recited in the rejected claims. Attention is directed to Figure 3, and in particular the elements CI1 and CI2 which constitute one binary data latch circuit, and the elements CI3 and CI4 which constitute another binary data latch circuit. Accordingly, the rejection under 35 USC §112, first paragraph, is traversed.

In response to the rejection under 35 USC §112, second paragraph, the informalities identified have been corrected herewith.

Turning now to the merits, Applicants respectfully traverse the outstanding rejection under 35 USC §102(e), because in Applicants' view the claimed invention clearly patentably define over the applied Mehrotra et al reference. In the following discussion, the differences between the claimed invention and Mehrotra et al are described.

First, FIG. 16 of Mehrotra et al and FIG. 3 of the present application will be compared. Both of these figures show a circuit for controlling the writing of data an a multi-flash memory device. To be more specific, the circuit enables data to be written in a large number of memory cells at a time.

To write data in the memory cells at a time, many pieces of data are initially input, and are internally latched for write control. After input of external data, an internal write operation and an internal verify operation are repeated, thereby controlling the threshold values of the memory cells.

In the case of Mehrotra et al, the data ("READ DATA BIT") read from the memory cells for a read-verify operation and the write data ("WRITE DATA BIT") initially sent from an external device are compared with each other. On the basis of this comparison, a determination is made to see whether or nor data has been read in the memory cell. The

result of this determination is stored in a latch circuit 721, and then output to signal line 731. When memory cells are determined as storing accurately-written data, those memory cells are set in the write prohibit state.

In the case of Mehrotra et al, two latch circuits are required: one is circuit 721 for storing a result of determination, and the other is circuit 190 for storing write data initially transmitted from an external device.

It should be noted, however, that the states of the memory cells are liable to vary. Even after a memory cell is determined as storing accurately-written data, the same memory cell may be regarded as being in the insufficiently written state. If this happens, an unnecessary data write operation is executed, giving adverse effects to the flash memory device. In actuality, noise in a memory cell array often gives rise to the phenomenon that the state of a memory cell is determined as having varied even though it remains the same.

In Applicants' invention, the data initially sent from an external device is latched in latch circuits (CI1, CI2, CI3 and CI4). When it is determined that data has been accurately written in memory cells, the latched data is changed to "0," thereby prohibiting a write operation.

As can be seen from the above, according to Applicants' invention the write data initially sent from an external device is modified each time a write-verify operation is executed. This feature is covered by each independent claim, which recites "for modifying stored data from said ith predetermines logic level to said first predetermined logic level ..." On the other hand, Mehrotra et al stores data initially sent from an external device in latch circuit 190.

In addition, according to Applicants' invention, write data that is set as "0" cannot be modified or changed. This is covered by each independent claim, which recites "for maintaining said stored data at said first predetermined logic level in the data storage portion storing the data of said first predetermined logic level." This function, i.e., the function of maintaining the write data that is set as "0," important to actual devices, clearly distinguishes over Mehrotra et al, which includes no disclosure of structure enabling this function.

As discussed in the foregoing, Claims 1-16, 19-32, 35-48, 51-64, 67-82, 85-100 and 103-116 disclose an invention fundamentally different from that of Mehrotra et al. Needless to say, the advantages attained by Applicants' invention differ from those of Mehrotra et al.

Consequently, in light of the present amendment, no further issues are believed to be outstanding, and the present application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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Please amend Claims 120, 121, 123, 125, 127, 129, 133, 139, 143 and 150 as follows:

120. (Amended) A multilevel nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a [program] circuit, coupled to said word lines and said bit line, for applying a write voltage to the word line of a selected memory cell, for applying a verify voltage to the word line of the selected memory cell to determine an actual threshold voltage of the selected memory cell while applying a pass voltage to remaining word lines of unselected memory fells in said NAND-cell unit to make the unselected memory cells act as transfer transistors, for applying a first level voltage to the bit line to change the threshold voltage of the selected memory cell in which it has been determined that the threshold voltage has not reached [to] a given threshold voltage level, said first level voltage being combined with said write voltage, and for applying a second level voltage to the bit line to maintain the threshold voltage of the

selected memory cell in which it has been determined that the threshold voltage has reached [to] said given threshold voltage level, said second level voltage being combined with said write voltage;

wherein said pass voltage is higher than said verify voltage.

121. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a plurality of word lines insulatively intersecting said [data transfer] bit lines;

a memory cell array coupled to said [data transfer] bit lines and said word lines, said memory cell array comprising a plurality of electrically programmable memory cells, each of said memory cells having at least three storage states;

a plurality of data latch circuits, each of said data latch circuits including plural binary data latch circuits and being coupled to a respective one of said [data transfer] bit lines, for storing write data in the form of combination of plural write binary data in a write operation, said write data being written into said memory cells, and for storing reach data in the form of a combination of plural read binary data in a read operation, said read data being read from said memory cells.

123. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a plurality of [data transfer] bit lines;

a plurality of word lines insulatively intersecting said [data transfer] bit lines;

a memory cell array coupled to said [data transfer] bit lines and said word lines, said memory cell array comprising a plurality of electrically programmable memory cells, each of said memory cells having at least three storage states;

a data conversion circuit, coupled to a plurality of data latch circuits, for converting plurality binary input data into plural internal write binary data; and

a plurality of data latch circuits, each including plural binary data latch circuits and being coupled to a respective one of said [data transfer] bit lines, for storing internal write data in the form of a combination of said plural internal write binary data in a write operation, said write data being written into respective memory cells.

125. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a plurality of [data transfer] bit lines;

a plurality of word lines insulatively intersecting said [data transfer] bit lines;

a memory cell array coupled to said [data transfer] bit lines and said word lines, said memory cell array comprising a plurality of electrically programmable memory cells, each of said memory cells having at least three storage states;

a data conversion circuit, coupled to a plurality of data latch circuits, for converting plural internal read binary data into plural binary output data; and

a plurality of data latch circuits, each including plural binary data latch circuits and being coupled to a respective one of said [data transfer] bit lines, for storing internal read data in the form of a combination of said plural internal read binary data in a read operation, said read data being read from respective memory cells.

127. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a plurality of [data transfer] bit lines;

a plurality of word lines insulatively intersecting said [data transfer] bit lines;

a memory cell array coupled to said [data transfer] bit lines[,] and said word lines, said memory cell array comprising a plurality of electrically programmable memory cells, each of said memory cells having at least three storage states;

a data conversion circuit, coupled to a plurality of data latch circuits, for converting plural binary input data into plural internal write binary data, and for converting plural internal read binary data into plural binary output data; and

a plurality of data latch circuits, each including plural binary data latch circuits and being coupled to a respective one of said [data transfer] bit lines, for storing internal write data in the form of a combination of said plural internal write binary data in a write operation, said write data being written into respective memory cells, and for storing internal read data in the form of a combination of said plural internal read binary data in a read operation, said read data being read from respective memory cells.

129. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having multi-levels storage states;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a word line selector coupled to said word lines for selecting the word line of a selected memory cell;

a data latch circuit coupled to said word lines for storing data, said data latch circuit including at least two binary data latch circuits;

a first bit line bias circuit coupled to said bit line for biasing said bit line dependent on the data stored in said data latch circuit; and

a second bit line bias circuit coupled to said bit line for biasing said bit line independent of the data stored in said data latch circuits.

133. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a [read] circuit, coupled to said word lines and said bit line, for applying one of at leat two read voltages to the word line of a selected memory cell to determine whether or not a threshold voltage of the selected memory cell is higher than said one of at least two read voltages while applying a pass voltage to remaining word lines of unselected memory cells in said NAND-cell unit to make the unselected memory cells act as transfer transistors;

wherein said pass voltage is higher than said at least two read voltages.

139. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a [verify] circuit, coupled to said word lines and said bit line, for applying one of at least two verify voltages to the word line of a selected memory cell to determine whether or not a threshold voltage of the selected memory cell reaches [to] one of said at least three threshold voltage levels while applying a pass voltage to remaining word lines of unselected memory cells in said NAND-cell unit to make the unselected memory cells act as transfer transistors;

wherein said pass voltage is higher than said at least two verify voltages.

143. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having multi-level storage states;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a word line selector coupled to said word lines for selecting the word line of a selected memory cell, the selected word line having applied thereto read voltages in a read operation, the remaining word lines of unselected memory cells in said NAND-cell unit having applied thereto a pass voltage to make unselected memory cells act as transfer transistors in said read operation, said pass voltage being higher than said read voltages; and

a bit line precharge circuit coupled to said bit line for charging said bit line at the beginning of said read operation.

150. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell; unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a [verify] circuit, coupled to said word lines and said bit line, for applying, to the word line of a selected memory cell, a first voltage in a first portion of a verify operation and a second voltage in second portion of said verify operation while applying, to remaining word lines of unselected memory cells in said NAND-cell unit, a third voltage in said first and second portions of said verify operation.

Please add new Claims 151-174 as follows:

--151. (New) A multi-level non-volatile semiconductor memory device comprising:

a plurality of memory cells, each being capable of having one of first, second, and third storage levels; and

a plurality of programming control circuits coupled to each of the memory cells,

wherein each of said programming control circuits is capable of storing in a data storage portion data of one of first, second, and third logic levels which define write voltage to be applied to a corresponding memory cell, for applying said write voltage to the corresponding memory cell according to the data stored in the data storage portion, for determining whether the corresponding memory cell has reached the second storage level only in case that the data stored in the data storage portion represents the second logic level,

for determining whether the corresponding memory cell has reached the third storage level only in case that the data stored in the data storage portion represents the third logic level, for modifying the stored data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the second storage level, for modifying the stored data from the third logic level to the first logic level if it has been determined that the corresponding memory cell has reached the third storage level, and for maintaining the stored data at the first logic level if the data storage portion has stored the data of the first logic level.

152. (New) The device according to claim 151, wherein the programming control circuits storing the data of the first logic level apply a first write voltage, which inhibits changes in the storage levels, to the corresponding memory cells.

153. (New) The device according to claim 152, wherein the programming control circuits storing the data of the second logic level apply a second write voltage, which promotes changes to the second storage level in the corresponding memory cells, to the corresponding memory cells, and the programming control circuits storing the data of the third logic level apply a third write voltage, which promotes changes to the third storage level in the corresponding memory cells, to the corresponding memory cells.

154. (New) The device according to claim 153, wherein said second write voltage is different from said third write voltage.

155. (New) The device according to claim 151, wherein each data storage portion includes two CMOS flip-flop circuits.

156. The device according to claim 151, further comprising data detectors for detecting whether all of said data storage portions have stored the data of the first logic level.

157. (New) The device according to claim 151, wherein plural of the memory cells store three-bit data.

158. (New) A multi-level non-volatile semiconductor memory device comprising:

a plurality of memory cells each being capable of having one of first second and third storage levels; and

a plurality of programming control circuits coupled to each of the memory cells,

wherein each of said programming control circuits is capable of storing first data of one of first and second logic levels in a first data storage portion and capable of storing second data of one of first and second logic levels in a second data storage portion, for applying a first write voltage to corresponding memory cell in case that the first data represents the first logic level in order to inhibit change in the storage level of the corresponding memory cell, for applying a second write voltage to the corresponding memory cell in case that the first data represents the second logic level in order to promote change in the storage level of the corresponding memory cell, for determining whether the corresponding memory cell has reached the second storage level only in case that the first data represents the second logic level and the second data represents the first logic level, for determining whether the corresponding memory cell has reached the third storage level only in case that the first data represents the second logic level and the second data represents the second logic level, for modifying the stored first data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the second storage level, for modifying the stored first data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the third

storage level, and for maintaining the stored first data at the first logic level if the first data storage portion has stored the first date of the first logic level.

159. (New) The device according to claim 158, wherein a voltage level of the second write voltage to be applied to the memory cell corresponding to the programming control circuit storing the second data of the first logic level is different from a voltage level of the second write voltage to be applied to the memory cell corresponding to the programming control circuit storing the second data of the second logic level.

160. (New) The device according to claim 158, wherein said first data storage portion includes a CMOS flip-flop circuit, and said second data storage portion includes a CMOS flip-flop circuit.

161. (New) The device according to claim 158, further comprising data detectors for detecting whether all of said first data storage portions have stored the first data of the first logic level.

162. (New) The device according to claim 158, wherein plural of the memory cells store three-bit data.

163. (New) A multi-level non-volatile semiconductor memory device comprising:

a plurality of memory cells, each being capable of having one of first, second and third storage levels; and

a plurality of programming control circuits coupled to each of the memory cells,

wherein each of said programming control circus is capable of storing in a data storage portion data of one of first, second, and third logic levels which define write voltage to be applied to a corresponding memory cell, for applying said write voltages to the corresponding memory cell according to the data stored in the data storage portion, for

determining whether the corresponding memory cell has reached the second storage level in case that the data stored in the data storage portion represents the second logic level, for determining whether the corresponding memory cell has reached the third storage level in case that the data stored in the data storage portion represents the third logic level, for modifying the stored data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the second storage level, for modifying the stored data from the third logic level to the first logic level if it has been determined that the corresponding memory cell has reached the third storage level, and for maintaining the data at the first logic level if the data storage portion has stored the data at the first logic level, and

wherein the programming control circuits storing said data of said second logic level determine only whether the corresponding memory cell has reached the second storage level and the programming control circuits storing said data of said third logic level determine only whether the corresponding memory cell has reached the third storage level.

164. (New) The device according to claim 163, wherein said programming control circuits storing the data of the first logic level apply a first write voltage which inhibits changes in the storage levels to the corresponding memory cells.

165. (New) The device according to claim 164, wherein said programming control circuits storing the data of the second logic level apply a second write voltage which promotes changes to the second storage level in the corresponding memory cells, to the corresponding memory cells, and said programming control circuits storing the data of the third logic level apply third write voltage which promotes changes to the third storage level in the corresponding memory cells, to the corresponding memory cells.

166. (New) The device according to claim 165, wherein said second write voltage is different from said third write voltage.

167. (New) The device according to claim 163, wherein each data storage portion includes two CMOS flip-flop circuits.

168. (New) The device according to claim 163, further comprising data detectors for detecting whether all of said data storage portions have stored the data of the first logic level.

169. (New) The device according to claim 163, wherein a couple of the memory cells stores three-bit data.

170. (New) A multi-level non-volatile semiconductor memory device comprising:

a plurality of memory cells, each being capable of having one of first, second and third storage levels; and

a plurality of programming control circuits coupled to each of the memory cells,

wherein each of said programming control circuits is capable of storing in a first data storage portion first data of one of first and second logic levels and of storing in a second data storage portion second data of one of first and second logic levels, for applying first write voltage to a corresponding memory cell in case that the first data represents the first logic level in order to inhibit change in the storage level of the corresponding memory cell, for applying second write voltage to the corresponding memory cell in case that the first data represents the second logic level in order to promote change in the storage level of the corresponding memory cell, for determining whether the corresponding memory cell has reached the second storage level in case that the first data represents the second logic level and the second data represents the first logic level, for determining whether the corresponding memory cell has reached the third storage level in case that the first data represents the second

logic level and the second data represent the second logic level, for modifying the stored first data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the second storage level, for modifying the stored first data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the third storage level, and for maintaining the stored first data at the first logic level if the first data storage portion has stored the first data of the first logic level, and

wherein the programming control circuits storing the first data of the second logic level and the second data of the first logic level determine only whether the corresponding memory cell has reached the second storage level, and the programming control circuits storing the first data of the second logic level and the second data of the second logic level determine only whether the corresponding memory cell has reached the third storage level.

171. (New) The device according to claim 170, wherein a voltage level of the second write voltage to be applied to the memory cell corresponding to the programming control circuit storing the second data of the first logic level is different from a voltage level of the second write voltage to be applied to the memory cell corresponding to the programming control circuit storing the second data of the second logic level.

172. (New) The Device according to claim 170, wherein said first data storage portion includes a CMOS flip-flop circuit, and said second data storage portion includes a CMOS flip-flop circuit.

173. (New) The device according to claim 170, further comprising data detectors for detecting whether all of said first data storage portions have stored the first data of the first logic level.

174. (New) The device according to claim 170, wherein a plural of the memory cells stores three-bit data.--